IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application	)		
No. 10/630,480	)	**For:**	**BUILT-IN SELF-TEST (BIST) ARCHITECTURE HAVING DISTRIBUTED INTERPRETATION AND GENERALIZED COMMAND PROTOCOL**
Averbuj et al.	)		
Examiner: Saqib Javaid Siddiqui	)		
Filed: July 29, 2003	)	**Group No.**	**2138**

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

A Final Office Action dated August 23, 2006 rejected all pending claims (claims 1-38) in the present application. A Notice of Appeal was submitted on February 23, 2007. Appellants' Appeal Brief is being filed herewith.

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Table of Contents

1. REAL PARTY IN INTEREST

The real party in interest is the assignee, QUALCOMM, Inc.

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals and/or interferences.

3. STATUS OF CLAIMS

Claims 1-38 are pending in the present application. Claims 1-24 and 26-38 stand rejected under 35 U.S.C. § 102(b). Claims 1-10, 12, 25 and 28 stands rejected under 35 U.S.C. § 103(a). Appellants appeal the rejections of claims 1-38.

4. STATUS OF AMENDMENTS

No amendments were filed subsequent to the final rejection.

5. SUMMARY OF CLAIMED SUBJECT MATTER

As stated in the background section of Appellants' specification, built-in self-test (BIST) units are now commonly incorporated into memory chips and other integrated circuits to test their functionality and reliability. For example, a BIST unit incorporated into a particular memory module operates by writing and reading various data patterns to and from the associated memory module to detect any possible memory faults. By comparing the data written and the data subsequently returned from the memory module, the BIST unit is able to determine whether any memory cell of the memory module is faulty.

The integrated BIST unit typically generates a variety of predetermined test patterns and asserts or deasserts an output signal based on the results of the memory test. A variety of algorithms may be used for detecting memory faults. For example, test patterns of all zeros, all ones, or a "checkerboard" pattern having alternating zeros and ones may be written throughout the memory cells. Moreover, the data may be written to the cells in any order, such as consecutively in an increasing or decreasing addressing scheme.

Thus, BIST units are commonly included in many types of integrated circuits that use or otherwise incorporate memory modules and operate according to some predetermined algorithm to verify the functionality of the internal chip circuitry. However, electronic devices typically comprise more than the internal circuitry of a single chip. Normally they are constructed from many integrated circuit chips and many supporting components mounted on a circuit board.

As the complexity of a typical computing device increases, the number of memory chips and other integrated circuits increases. For example, conventional computing devices typically include a plurality of the memory modules, which are often of different types. The memory modules with a single computing device may include various combinations of random access memory (RAM), read-only memory (ROM), Flash memory, dynamic random access memory (DRAM), and the like. These various types of memory modules often require different testing procedures, and have different bit densities, access speeds, addressing requirements, access protocols, and other particularities. As a result, a typical computing device may have a respective BIST unit for each memory module, and each BIST unit may be particularized to test the associated memory module.

The present invention is directed to a distributed, hierarchical BIST architecture for testing the operation of one or more memory modules. The architecture includes three tiers of abstraction: a centralized BIST controller, a set of sequencers, and a set of memory interfaces coupled to memory modules. The BIST controller provides centralized, high-level control over the testing of the modules. The sequencers receive the high-level commands from the BIST controller. The memory interfaces handle specific interface requirements for each of the memory modules.

As required by 37 C.F.R. § 41.37(c)(1)(v), a summary of claimed subject matter immediately follows. The references to the specification refer only to embodiments of the invention. The invention is defined by the claims. Accordingly, these references to the specification are not meant to limit the scope of the claims at issue in any way but are only provided because they are mandated by 37 C.F.R. § 41.37(c)(1)(v). All references are to Appellants' specification.

1. A system comprising:

a centralized built-in self-test (BIST) controller (page 5, line 12; page 6, line 29) that stores an algorithm (page 5, line 16) for testing a plurality of memory modules (page 5, line 15), wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol (page 5, lines 18-19); and

a plurality of distributed sequencers (page 5, lines 13-14) that interpret the commands based on the command protocol (page 5, lines 26-27) and apply the generalized commands to the memory modules (page 9, lines 26-29), each sequencer being associated with one or more memory modules operating on a common clock domain (page 6, lines 6-13), wherein at least two of the sequencers are associated with memory modules operating on different clock domains (page 6, lines 1-12).

26. A device comprising:

centralized built-in self-test (BIST) control means (page 5, line 12; page 6, line 29) for issuing commands that conform to a generalized command protocol (page 5, lines 18-19) and define a BIST algorithm (page 5, line 16) for testing a plurality of distributed memory modules having different timing requirements and physical characteristics (page 5, lines 15 and 19-21); and

distributed means for interpreting the commands (page 5, lines 13-14) and applying the commands to the memory modules in accordance with timing requirements and physical characteristics of the memory modules (page 5, lines 19-21), said distributed means including a plurality of sequencers, each sequencer being associated with one or more memory modules operating on a common clock domain (page 6, lines 6-13), wherein at least two of the sequencers are associated with memory modules operating on different clock domains (page 6, lines 1-12).

28. A method comprising:

directing application of an algorithm (page 5, line 16) from a centralized built-in self-test (BIST) controller (page 5, line 12; page 6, line 29) by issuing generalized commands that conform to a command protocol (page 5, lines 18-19) to test a plurality of memory modules (page 5, lines 15 and 19-21; page 18, lines 4-7); and

interpreting the commands (page 5, lines 13-14; page 18, lines 7-11) with a distributed set of sequencers to apply the commands as one or more sequences of memory operations in accordance with the command protocol page 5, lines 19-21), each sequencer being associated with one or more memory modules operating on a common clock domain (page 6, lines 6-13), wherein at least two of the sequencers are associated with memory modules operating on different clock domains (page 6, lines 1-12).

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following issues are presented for review:

A. Whether claims 1-24 and 26-38 are unpatentable under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,995,731 to Crouch et al.

B. Whether claims 1-10, 12, 25 and 28 are unpatentable under 35 U.S.C. § 103(a) as being anticipated by U.S. Patent No. 6,347,056 to Ledford et al.

7. ARGUMENT

A. Claims 1-24 and 26-38 Rejected under 35 U.S.C. § 102(b)

Claims 1-24 and 26-38 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,995,731 to Crouch et al. (hereinafter "Crouch"). Appellants respectfully submit that claims 1-24 and 26-38 are patentably distinct from Crouch and request that this rejection be withdrawn.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP § 2131 (citing Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). "The identical invention must be shown in as complete detail as is contained in the ... claim." Id. (citing Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). In addition, "the reference must be enabling and describe the applicant's claimed invention sufficiently to have placed it in possession of a person of ordinary skill in the field of the invention." In re Paulsen, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

Claim 1 recites "a centralized built-in self-test (BIST) controller . . . and a plurality of distributed sequencers." Crouch does not disclose both of these claim elements. The Office Action of August 23, 2006 (hereinafter, "Office Action") asserts that "Crouch et al. teaches . . . a plurality of sequencers that interpret the commands based on the command protocol." Office Action, page 4. To support this assertion, the Office Action points to column 2, lines 5-10 of Crouch. This portion of Crouch states "[a] similar set of trade-offs can be applied to a memory BIST architecture. In this case, the memory test sequencer, stimulus generator, and comparator logic are all embedded within a single chip. Access to all of the individual memory arrays is provided." Office Action, page 3 (quoting Crouch, col. 2, lines 5-10). Regarding this cited passage of Crouch, the Office Action states "since more then [sic] one chip can be tested at one time, there will be a plurality of sequencers." Office Action, page 3. Appellants respectfully disagree with this conclusion set forth by the Office Action.

Crouch states "embedded memory is generally placed along one side of the chip, or in one physical area. The embedded memory is then tested by one of several methods." Crouch, col. 1, lines 23-26. One "method of testing [the embedded memory] that can be used is an internal embedded Memory Built-In Self-Test (MBIST or memory BIST)." Crouch, col. 1, lines 31-33. From these cited passages, Crouch discloses memory "along on side of the [single] chip." As such, "the memory test sequencer" previously cited above is also "within [the single] chip." In other words, Crouch is merely disclosing a single chip with "embedded memory along one side of the chip" and "the memory test sequencer . . . within . . . [the] chip." Id. Crouch further discloses "there is more opportunity and need to embed ever greater quantities of memory on single integrated circuit die." Crouch, col. 1, lines 39-40. Thus, Crouch's statement of "all of the individual memory arrays" discloses that all of the memory arrays are "on single integrated circuit die" along with "the [single] memory test sequencer." Id.

In contrast, claim 1 recites "a centralized built-in self-test (BIST) controller . . . for testing a plurality of memory modules . . . [and] stores . . . commands . . . and a plurality of distributed sequencers that . . . apply the . . . commands to the memory modules." The BIST controller of claim 1 is centralized. As such, the plurality of memory modules tested by the BIST controller is centralized as well as the plurality of distributed sequencers. Crouch does not disclose "a centralized built-in self-test (BIST) controller . . . and a plurality of distributed

sequencers." As previously mentioned, Crouch merely discloses "the [single] memory test sequencer . . . [is] embedded within a single chip." Crouch, col. 2, lines 7-9. The Office Action's assertion that "since more then [sic] one chip can be tested at one time, there [are] a plurality of sequencers" does not support the assertion that Crouch discloses "a plurality of sequencers." Crouch discloses a single sequencer on a single chip while claim 1 recites "a centralized . . . (BIST) controller . . . and a plurality of distributed sequencers."

Further, the Office Action points to Figure 2, element 210 in support of the assertion that Crouch discloses "a centralized built-in self-test (BIST) controller." See Office Action, page 4. Appellants respectfully disagree.

Figure 2 of Crouch illustrates "multiple memory BIST controllers." Crouch, col. 5, line 52. Figure 2 further illustrates "[a]n integrated circuit 200 contains two memories 215, 225 with an associated BIST controller per memory." Crouch, col. 5, lines 54-56. Multiple BIST controllers that are associated with memory does not disclose "a centralized built-in self-test (BIST) controller" as claimed by Appellants. In other words, Crouch describes a typical memory testing architecture in which a BIST controller is provided for each memory module. This approach is expensive in terms of area and overhead for the BIST controllers during testing. Crouch also discloses "the BIST modules should be staged in a combination parallel-sequential manner." Crouch, col. 8, lines 2-3. However, the "parallel-sequential" refers to an architecture in which a BIST controller is provided for each memory module and does not disclose "a centralized . . . (BIST) controller."

The Office Action points to Figure 2, elements 210 and 225 as supporting the assertion that Crouch discloses "a plurality of sequencers." Appellants respectfully disagree. Element 210 in Figure 2 of Crouch is labeled a "BIST controller" while element 225 is labeled "memory." A BIST controller and memory does not disclose "a plurality of sequencers that interpret the commands based on the command protocol." Instead, a "BIST controller creates the test stimulus and the testing sequencing for all of the embedded memory arrays." Crouch, col. 1, lines 34-36. Creating the test stimulus and testing sequencing does not disclose "interpret[ing] the commands based on the command protocol." Further, Crouch states:

> FIG. 2 is a block diagram that illustrates an integrated circuit architecture with multiple memory BIST controllers to control memory testing of a corresponding plurality of memory arrays. An integrated circuit 200

> contains two memories 215, 225 with an associated BIST controller per memory.

Crouch, col. 5, lines 51-55.

It appears that the Office Action is again asserting that "multiple memory BIST controllers" discloses "a plurality of sequencers." As previously explained, BIST controllers disclosed in Crouch are not the same as sequencers claimed by Appellants. Crouch states that "BIST controller creates the test stimulus and the testing sequencing for all of the embedded memory arrays." Crouch, col. 1, lines 34-36. However, as also previously explained, creating the test stimulus and testing sequencing does not disclose "interpret[ing] the commands based on the command protocol."

Claim 1 also recites "wherein at least two of the sequencers are associated with memory modules operating on different clock domains." Crouch does not disclose this claim element. Instead, Crouch states:

> One of the key cost items to testing memories is a retention test. This test starts by loading sequential logic with a particular set of logic values (referred to as "DATA"), stopping the clock for a period of time, and then verifying the ability of the sequential logic to retain the first set of logic values. A second set of logic values, that are generally the complement of the first set ("DATABAR"), is then applied to the sequential logic, the clock is again stopped and re-started, and the sequential logic is verified again.

Crouch, col. 2, lines 24-32.

Crouch further states "that all memory arrays can be retention tested simultaneously." Crouch, col. 3, lines 5-6. Retention testing all memory arrays simultaneously does not disclose "wherein at least two of the sequencers are associated with memory modules operating on different clock domains." In fact, testing all the memory arrays simultaneously discloses that all the memory arrays are on the same clock domain.

The retention test of Crouch disclosed above simply discloses "stopping the clock . . . verifying the ability of the sequential logic to retain the first set of logic values . . . [applying] a second set of logic values . . . [stopping] the clock . . . again . . . and [verifying] the sequential logic." Stopping and starting the clock does not disclose "wherein at least two of the sequencers are associated with memory modules operating on different clock domains" as claimed by

Appellants. Crouch merely discloses the stopping and starting of the clock with no disclosure of "memory modules operating on different clock domains."

Crouch also states "creating an independent memory BIST controller for each distributed memory array . . . and, if the memories are of different sizes (data width and address space), or in different frequency domains, there may not be a single point in time that a retention pause can be applied." Crouch, col. 4, lines 42-51. The Office Action points to this passage of Crouch to support the assertion that Crouch discloses "the memory modules . . . can be of different clock domains." Office Action, page 3. Appellants respectfully disagree with this assertion. As previously mentioned, claim 1 recites "wherein at least two of the sequencers are associated with memory modules operating on different clock domains." However, Crouch discloses "an independent memory BIST controller for each distributed memory array . . . and, [the memory arrays may be] in different frequency domains." There is no disclosure in the cited passages of Crouch of "at least two of the sequencers . . . associated with memory modules operating on different clock domains." A BIST controller does not disclose "at least two of the sequencers." In addition, the Office Action merely infers that "different frequency domains" discloses "different clock domains." As such, Appellants submit that Crouch does not disclose "wherein at least two of the sequencers are associated with memory modules operating on different clock domains."

In view of the foregoing, Appellants submit that claim 1 is patentably distinct from Crouch. Accordingly, Appellants respectfully request that the rejection of claim 1 be withdrawn.

Claims 2-24 depend either directly or indirectly from claim 1. As such, Appellants submit that claims 2-24 are patentably distinct from Crouch for at least the same reasons as those presented above in connection with claim 1. Accordingly, Appellants respectfully request that the rejection of claims 2-24 be withdrawn because Crouch does not disclose each and every element of claim 1.

Claim 26 includes claim elements that are similar to claim 1. As such, Appellants submit that claim 26 is patentably distinct from Crouch for at least the same reasons as those presented above in connection with claim 1. Accordingly, Appellants respectfully request that the rejection of claim 26 be withdrawn.

Claim 27 depends directly from claim 26. As such, Appellants submit that claim 27 is patentably distinct from Crouch for at least the same reasons as those presented above in connection with claim 26. Accordingly, Appellants respectfully request that the rejection of claim 27 be withdrawn because Crouch does not disclose each and every element of claim 26.

Claim 28 includes claim elements that are similar to claim 1. As such, Appellants submit that claim 28 is patentably distinct from Crouch for at least the same reasons as those presented above in connection with claim 1. Accordingly, Appellants respectfully request that the rejection of claim 28 be withdrawn.

Claims 29-38 depend either directly or indirectly from claim 28. As such, Appellants submit that claims 29-38 are patentably distinct from Crouch for at least the same reasons as those presented above in connection with claim 28. Accordingly, Appellants respectfully request that the rejection of claims 29-38 be withdrawn because Crouch does not disclose each and every element of claim 28.

B. Claims 1-10, 12, 25 and 28 Rejected under 35 U.S.C. § 103(a)

Claims 1-10, 12, 25 and 28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,347,056 to Ledford et al. (hereinafter "Ledford"). Appellants respectfully submit that claims 1-10, 12, 25 and 28 are patentably distinct from Ledford and request that this rejection be withdrawn.

The M.P.E.P. states that:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.
>
> The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of

> reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

M.P.E.P. § 2142.

Claim 1 recites "wherein at least two of the sequencers are associated with memory modules operating on different clock domains." Ledford does not teach or suggest this claim element. Instead, Ledford states "[t]he multiple memories may be different or the same regarding type, size, data widths, etc." Ledford, Abstract, lines 7-10. The Office Action appears to use this broad statement to support the assertion that Ledford teaches "memory modules operating on different clock domains." Simply stating that memory modules may be "different or the same regarding type, size, data widths, etc." does not teach or suggest that the "memory modules [are] operating on different clock domains." In fact, Ledford focuses on the particular size of the memory modules. For instance, Ledford states:

> [F]our memory array configurations are shown having four different sizes. It should be well understood that the present invention may be implemented with any number, type and size of memory arrays. For example, all memory arrays may have the same size and the present invention may also be practiced using only a single memory array.

Ledford, col. 3, lines 6-11.

This cited passage of Ledford illustrates that Ledford focuses its teachings on different sizes of memory modules. There is no teaching or suggestion of these "memory modules operating on different clock domains." It appears that the Office Action has merely inferred that Ledford teaches "different clock domains" because Ledford teaches that memory modules may be different regarding "number, type and size." Id. However, as previously explained, "number, type and size" does not teach or suggest "operating on different clock domains."

In view of the foregoing, Appellants submit that claim 1 is patentably distinct from Ledford. Accordingly, Appellants respectfully request that the rejection of claim 1 be withdrawn because Ledford does not teach or suggest every claim element of claim 1.

Claims 2-10, 12 and 25 depend either directly or indirectly from claim 1. As such, Appellants submit that claims 2-10, 12 and 25 are patentably distinct from Ledford for at least the same reasons as those presented above in connection with claim 1. Accordingly, Appellants respectfully request that the rejection of claims 2-10, 12 and 25 be withdrawn because Crouch does not teach or suggest every element of claim 1.

Claim 28 includes claim elements that are similar to claim 1. As such, Appellants submit that claim 28 is patentably distinct from Ledford for at least the same reasons as those presented above in connection with claim 1. Accordingly, Appellants respectfully request that the rejection of claim 28 be withdrawn because Ledford does not teach or suggest every claim element of claim 28.

Respectfully submitted,

Dated: May 23, 2007

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CLAIMS APPENDIX

Listing of Claims involved in the appeal:

1. A system comprising:

a centralized built-in self-test (BIST) controller that stores an algorithm for testing a plurality of memory modules, wherein the BIST controller stores the algorithm as a set of generalized commands that conform to a command protocol; and

a plurality of distributed sequencers that interpret the commands based on the command protocol and apply the generalized commands to the memory modules, each sequencer being associated with one or more memory modules operating on a common clock domain, wherein at least two of the sequencers are associated with memory modules operating on different clock domains.

2. The system of claim 1, wherein the generalized commands specify the algorithm in accordance with the command protocol and without regard to timing requirements of the memory modules.

3. The system of claim 1, wherein the generalized commands specify the algorithm without regard to physical characteristics of the memory modules.

4. The system of claim 1, wherein each of the generalized commands includes a sequencer identifier that identifies one or more of the sequencers to process the respective command and apply the command to the memory modules.

5. The system of claim 4, wherein the sequencer identifier comprises a broadcast identifier to indicate that the generalized command is to be interpreted and applied by all of the distributed sequencers.

6. The system of claim 4, wherein the sequencer identifier comprises a unicast identifier that identifies a specific one of the sequencers to interpret and apply the generalized command to the respective memory modules of the identified sequencer.

7. The system of claim 4, wherein the command protocols defines each of the generalized commands to include an operational code selected from a set of defined operational codes and a set of associated parameters.

8. The system of claim 7, wherein the set of defined operational codes includes an operational code that directs the sequencers to selectively enable and disable a BIST mode during which the sequencers ready the memory modules for testing by isolating the memory modules from address and data lines used during normal operation.

9. The system of claim 7, wherein the set of defined operation codes includes an operational code that directs the sequencers to apply a sequence of one or more memory operations over a range of addresses specified by the parameters.

10. The system of claim 9, wherein the parameters include a single-row (SR) field to direct the sequencers to apply the memory operations for all columns of the memory module of the respective memory modules for the sequencers that has a largest column-bit option while maintaining a row address at zero.

11. The system of claim 9, wherein the parameters include an invert bits field to direct the sequencers to invert data defined by the parameters for each row and column matrix of the memory modules when applying the memory operations.

12. The system of claim 9, wherein the parameters include a rippling row field to direct the sequencers to apply the memory operations to the memory modules in a column-wise fashion by holding a column address for each of the memory modules constant and rippling a row address for each of the memory modules.

13. The system of claim 9, wherein the parameters include an invert rows field to direct the sequencers to invert data defined by the parameters for neighboring rows of the memory modules when applying the memory operations.

14. The system of claim 9, wherein the parameters include an invert columns field to direct the sequencers to invert data defined by the parameters for neighboring columns of the memory modules when applying the memory operations.

15. The system of claim 9, wherein the parameters include a plurality of operational fields to direct the sequencers to apply multiple memory operations to each of memory addresses of the memory modules.

16. The system of claim 9, wherein the parameters include a default data in field that directs the sequencers to apply an input data value to the memory modules during a read operation.

17. The system of claim 7, wherein the set of defined operation codes includes an operational code that directs the sequencers to execute a defined memory operation to a specific address specified by the parameters.

18. The system of claim 7, wherein the set of defined operational codes includes an operational code that directs the sequencers to test a particular one of the memory modules.

19. The system of claim 7, wherein the parameters include a failure analysis field to direct the sequencers to selectively toggle between a failure analysis mode and a BIST mode.

20. The system of claim 19, wherein when operating within the failure analysis mode a memory identification field of the parameters directs the sequencers to select data from a specific

one of the memory modules for failure analysis and a bus slice field that indicates a portion of a multiplexed data bus from the selected memory module to be used for failure analysis.

21. The system of claim 7, wherein the set of defined operational codes includes an operational code that directs at least one of the distributed sequencers to apply a memory test algorithm stored within that sequencer.

22. The system of claim 1, further comprising a plurality of memory interfaces coupled between the sequencers and the memory modules, wherein the memory interfaces apply the commands to the memory modules under the direction of the sequencers and in accordance with physical characteristics of the memory module.

23. The system of claim 1, wherein BIST controller issues the commands to the sequencers in parallel for application to the memory modules.

24. The system of claim 1, wherein the sequencers apply the commands to the respective memory modules in accordance with timing requirements of the memory modules.

25. The system of claim 1, wherein each of the sequencers comprises:

a plurality of command controllers that implement the commands in accordance with a command protocol; and

a command parser to parse each of the commands to identify an operational code and a set of parameters based on the command protocol, wherein the command parser selectively invokes the command controllers based on the operational codes of the commands received from the BIST controller.

26. A device comprising:

centralized built-in self-test (BIST) control means for issuing commands that conform to a generalized command protocol and define a BIST algorithm for testing a plurality of distributed memory modules having different timing requirements and physical characteristics; and

distributed means for interpreting the commands and applying the commands to the memory modules in accordance with timing requirements and physical characteristics of the memory modules, said distributed means including a plurality of sequencers, each sequencer being associated with one or more memory modules operating on a common clock domain, wherein at least two of the sequencers are associated with memory modules operating on different clock domains.

27. The device of claim 26, wherein the distributed means includes interface means for generating translated address and data signals based on the physical characteristics of the memory modules to apply the BIST algorithm to the memory modules.

28. A method comprising:

directing application of an algorithm from a centralized built-in self-test (BIST) controller by issuing generalized commands that conform to a command protocol to test a plurality of memory modules; and

interpreting the commands with a distributed set of sequencers to apply the commands as one or more sequences of memory operations in accordance with the command protocol, each sequencer being associated with one or more memory modules operating on a common clock domain, wherein at least two of the sequencers are associated with memory modules operating on different clock domains.

29. The method of claim 28, wherein the generalized commands specify the algorithm without regard to physical characteristics and timing requirements of the memory modules.

30. The method of claim 28, wherein directing application of the algorithm comprises issuing each of the commands to include a sequencer identifier that identifies one or more of the sequencers to process the command and apply the command to the respective memory modules.

31. The method of claim 30, wherein the sequencer identifier comprises one of a broadcast identifier indicating that the command is to be interpreted and applied by all of the distributed sequencers and a unicast identifier that identifies a specific one of the sequencers to interpret the command.

32. The method of claim 28, wherein directing application of the algorithm comprises issuing each of the commands to include an operational code selected from a set of defined operations codes and a set of associated parameters.

33. The method of claim 32, wherein the set of defined operational codes includes an operational code that directs the sequencers to selectively enable and disable a BIST mode during which the sequencers ready the memory modules for testing by isolating the memory modules from address and data lines used during normal operation.

34. The method of claim 32, wherein the set of defined operation codes includes an operational code that directs the sequencers to apply a sequence of one or more memory operations over a range of addresses specified by the parameters.

35. The method of claim 32, wherein the set of defined operation codes includes an operational code that directs the sequencers to execute a defined memory operation to a specific address specified by the parameters.

36. The method of claim 32, wherein the set of defined operation codes includes an operational code that directs the sequencers to test a particular one of the memory modules.

37. The method of claim 33, wherein the set of defined operational codes includes an operational code that directs at least one of the distributed sequencers to apply a memory test algorithm stored within that sequencer.

38. The method of claim 29, wherein issuing an algorithm comprises issuing the commands to the sequencers in parallel for application to the memory modules.

EVIDENCE APPENDIX

NONE.

RELATED PROCEEDINGS APPENDIX

NONE.